AMENDMENT TO THE CLAIMS

Please add new claims 18-32 as follows:

18. (New) A system comprising:

a first serial device having n ports, each port supporting a serial communications path that carries, a data protection code within data transmissions on the serial communications path;

an on-chip memory located in the first serial device that receives a packet and the received packet's associated data protection code from the serial communications path; and

an integrity apparatus that uses the received, associated data protection code for data-integrity checking of the received packet that is in the on-chip memory.

19. (New) The system according to claim 18 wherein n comprises one or more.

20. (New) The system according to claim 18, further comprising:

a data storage device operatively coupled to the first serial device; and

a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device in a serial communications path in order to transfer data between the first and second serial devices through the serial communications path.

21. (New) The system according to claim 18, further comprising:

an off-chip memory operatively coupled to the on-chip memory and the integrity apparatus; and

a verification circuit within the integrity apparatus that verifies the data protection code while moving the received packet from the on-chip memory to the off-chip

memory.

22. (New) The system according to claim 21, wherein the integrity apparatus checks and strips away the data protection code while moving the received packet to the off-chip memory, the system further comprising:

a data protection code generation circuit that generates and appends a second data protection code to the data as the data are moved from the off-chip memory to the on-chip memory.

23. (New) The system according to claim 21, wherein a data packet devoid of a data protection code is held in the off-chip memory, the system further comprising:

a data protection code generator that generates data protection code based on the data packet from the off-chip memory as the data packet is moved into a data-packet buffer, and that places the generated data protection code into the on-chip memory with the data packet; and

a transmitter that transmits the data packet, including the generated data protection code, onto the communications path.

24. (New) A data storage device, comprising:

a storage medium;

a serial device having n ports, each port supporting a serial communications path, each serial communications path carrying a data protection code within data transmissions on the serial communications path, the serial device operatively coupled to the storage medium to communicate data;

an on-chip memory located on-chip in the serial device that receives a packet and the received packet's associated

data protection code from the serial communications path; and

an integrity apparatus that uses the received associated data protection code for data-integrity checking of the received packet that is in the on-chip memory.

25. (New) The data storage device according to claim 24, further comprising:

an off-chip memory operatively coupled to the on-chip memory and the integrity apparatus; and

a verification circuit within the integrity apparatus that verifies the data protection code while moving the received packet from the on-chip memory to the off-chip memory.

26. (New) A method comprising:

supporting a serial communications path on each of n ports of a first serial device;

receiving a packet from the serial communications path, the received packet including a data protection code that is based on other data in the received packet;

storing the received packet, including the data protection code, into a buffer;

moving the received packet to a separate memory that is separate from the buffer; and

checking the received packet for accuracy by verifying the data protection code while moving the received packet to the separate memory.

27. (New) The method according to claim 26, wherein receiving further comprises:

checking the received packet for accuracy by verifying the data protection code while receiving the received packet

from the communications path.

28. (New) The method according to claim 27, further comprising:
transferring data through the serial communications path between a data storage device that is operatively coupled to the first serial device and a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device by the serial communications path.

29. (New) The method according to claim 27, further comprising:
placing a packet that is to be transmitted into an on-chip buffer;
generating the data protection code based on data in the packet to be transmitted; and
transmitting the packet to be transmitted, including the data protection code, onto the serial communications path.

30. (New) The method according to claim 29, wherein placing comprises:
generating parity for data in the packet to be transmitted;
adding the parity to the data in the packet to be transmitted; and
wherein moving comprises:
stripping away the data protection code while moving the received packet to the separate memory.

31. (New) A system comprising:
a serial device having n ports, each port supporting a serial communications path, each serial communications path coupling a data protection code within data transmissions on the serial communications path;
a buffer that receives, from the serial communications path, a

packet that includes a data protection code;

an off-chip memory separate from the buffer;

means for moving the received packet from the buffer to the off-chip memory and checking the received packet for accuracy by verifying the data protection code while moving the received packet to the off-chip memory.

32. (New) The system according to claim 31, wherein the means for moving further comprises:

means for stripping away the data protection code as the packet is checked and moved to the off-chip memory.